REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 3-9 and 15-24 are in this application. Claims 1-2 and 10-14 have been cancelled. Claims 15-24 have been added. Claims 3-9 have been allowed.

The Examiner objected to the drawings under 37 CFR §1.83(a) in view of the limitations recited in claims 10-14, rejected claims 10-14 under 35 U.S.C. §112, first paragraph, and rejected claims 10-14 under 35 U.S.C. §112, second paragraph. As noted above, claims 10-14 have been cancelled.

The Examiner rejected claims 10-14 under 35 U.S.C. §103(a) as being unpatentable over Klein (U.S. Patent No. 4,205,330) in view of Takagi (U.S. Patent No. 4,003,071). As noted above, claims 10-14 have been cancelled. With respect to new claim 15, this claim recites, in relevant part:

> "a first transistor having:
>
> "a first channel region that contacts and lies between the first source and drain regions, the first channel region having a first channel length;
>
> "a layer of first gate oxide formed over the first channel region, the layer of gate oxide having a first thickness; and
>
> "the first transistor conducting more than a leakage current when the first gate, the first source, and the first semiconductor region are connected to a same potential;
>
> "a second transistor having:
>
> "a second channel region that contacts and lies between the second source and drain regions, the second channel region having a second channel length that is greater than the first channel length;
>
> "a layer of second gate oxide formed over the second channel region, the layer of second gate oxide having a second thickness that is greater than the first thickness; and
>
> "the second transistor being substantially non-conductive when the gate of the second transistor, the second source, and the second semiconductor region are connected to a same potential."

In rejecting prior claim 10, the Examiner pointed to the Klein reference as teaching a depletion mode transistor and an enhancement mode transistor, where region 30a shown in FIG. 4 Klein constitutes the first channel required by the claims, and gate oxide layer 29a shown in FIG. 4 of Klein constitutes the layer of first gate oxide required by the claims. In addition, the Examiner pointed to region 30 shown in FIG. 4 Klein as constituting the second channel required by the claims, and gate oxide layer 29 shown in FIG. 4 of Klein as constituting the layer of second gate oxide required by the claims.

The Examiner noted that channel region 30a in FIG. 4 of Klein is shorter than channel region 30, but conceded, in rejecting claim 11, that the Klein reference does not disclose that the layer of first gate oxide 29a has a first thickness and the layer of second gate oxide 29 has a second thickness that is greater than the first thickness of the layer of first gate oxide 29a.

As a result, the Examiner pointed to the Takagi reference as teaching a depletion mode transistor and an enhancement mode transistor, where gate insulating film 66 of depletion transistor 63 shown in FIG. 6A of Takagi constitutes the layer of first gate oxide required by the claims, and gate insulating film 65 of enhancement transistor 62 shown in FIG. 6A of Takagi constitutes the layer of second gate oxide required by the claims.

The Examiner noted that gate insulating film 65 is thicker than gate insulating film 66. In addition, the Examiner, pointing to column 8, lines 17-34 of Takagi, noted that Takagi teaches that the thickness of gate insulation film 66 allows the formation of an impurity diffused layer, whereas the thickness of gate insulation film 65 is too thick and thereby prevents the formation of an impurity diffused layer.

More specifically, Takagi teaches a single implantation step that forms the source and drain regions 68 and 69 of the enhancement and depletion transistors 62 and 63, respectively, where the single implantation step also forms impurity diffused

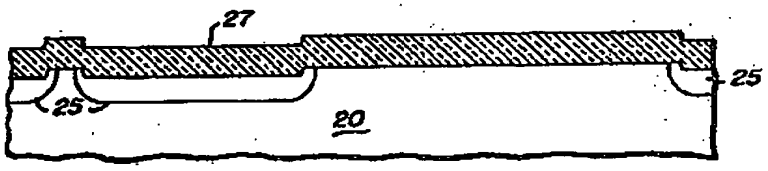
layer 70 in depletion transistor 63. (See column 8, lines 9-17 of Takagi.) As noted by the Examiner, no impurity diffused layer is formed in the channel region of enhancement transistor 62 because gate insulation film 65 is too thick.

The Examiner then appears to argue that it would be obvious to modify Klein to form gate oxide layer 29 shown in FIG. 4 of Klein to be thicker than gate oxide 29a so that a single implant could be used to form channel region 30a (while at the same time forming the source and drain regions of the enhancement and depletion transistors).

The Examiner argued that one skilled in the art would be motivated to modify Klein in this fashion because to do so would allow the enhancement and depletion transistors of Klein to be formed using fewer manufacturing steps. However, as set forth below, modifying the Klein reference as suggested by the Examiner does not result in fewer manufacturing steps, but instead requires significantly more manufacturing steps.

To illustrate this, applicant has inserted a number of annotated drawings which show the additional manufacturing steps which would be required to realize the modification suggested by the Examiner. Klein teaches the initial manufacturing steps illustrated in FIGS. 3a-3c, of which FIG. 3c is illustrated below.

Fig_3c



However, to form the gate oxide layers with different thickness as suggested by the Examiner, the first step following FIG. 3c is to mask and etch oxide layer 27 (see the reference label in FIG. 3c of Klein) to form a first window A as shown below in annotated FIG. 3c1 where the to-be-formed enhancement transistor is to be formed.

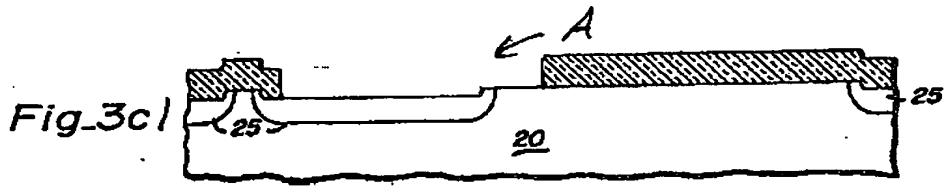


Fig_3c1

Following this, as shown below in annotated FIG. 3c2, a gate oxide film B is formed for the enhancement transistor by thermal oxidation to be less than the final desired thickness of the film. (See column 5, lines 58-62; and from column 7, line 67 to column 8, line 2 of Takagi.)

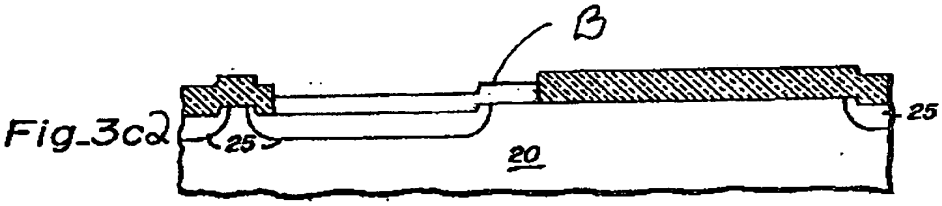


Fig_3c2

After this, oxide layer 27 must be masked and etched to form a second window C as shown below in annotated FIG. 3c3.

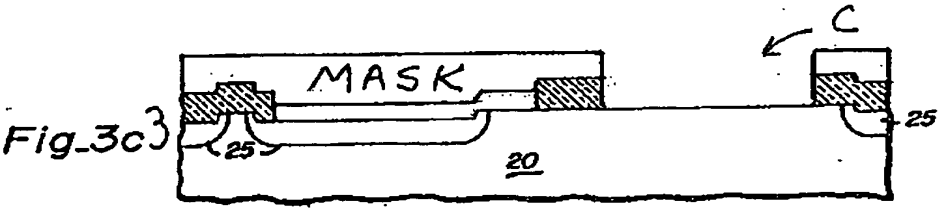
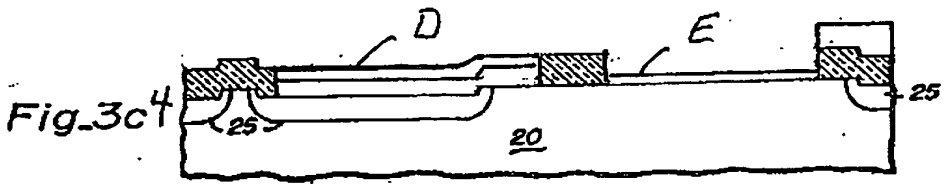
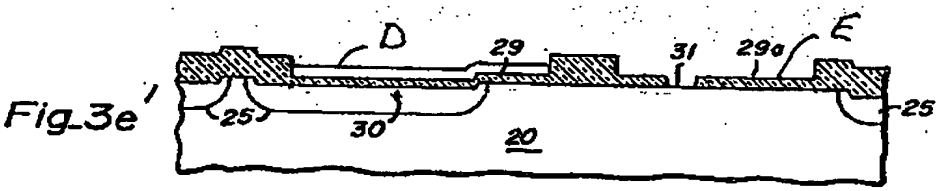


Fig_3c3

Next, as shown below in annotated FIG. 3c4, the thickness of gate oxide film B of the enhancement transistor is increased to form a gate oxide film D with the final thickness, while a gate oxide film E is formed for the depletion transistor. (See column 5, lines 58-62 of Takagi.)



Once the thicker gate oxide layer D for the enhancement transistor and the thinner gate oxide layer E for the depletion transistor have been formed, the process can revert back to the original teachings of Klein where, as shown below in FIG. 3e', hole 31 is formed in gate oxide layer 29a (E) prior to the deposition of the polysilicon layer.



Thus, when the polysilicon layer is subsequently etched, as shown in FIG. 3f of Klein to form gates 32 and 34, the following implant step can form region 30a shown in FIG. 4 of Klein in the manner taught by Takagi.

However, as the above annotated drawings illustrate, the method of forming region 30a suggested by the Examiner does not result in fewer manufacturing steps, but instead results in a net increase of three additional manufacturing steps. Thus,

one skilled in the art would not be motivated to form the enhancement and depletion transistors of Klein with the different gate oxide thicknesses of Takagi because to do so would increase production costs.

As a result, claim 15 is patentable over the Klein reference in view of the Takagi reference. In addition, since claims 16-24 depend either directly or indirectly from claim 15, claims 16-24 are patentable over the Klein reference in view of the Takagi reference for the same reasons as claim 15.

Thus, for the foregoing reasons, it is submitted that the application is in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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